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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,391	09/30/2003	Sheng-Hua Chen	TOP 334	3756

23995 7590 07/16/2004

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,391	CHEN ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1-4 and 7* is/are rejected.

7)☒ Claim(s) *5,6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on line 10 of page 15, "node an Is grounded" is not understood what it exactly means. Appropriate correction is required.

Claim Objections

2. Claims 1-8 are objected to because of the following informalities: on line 17 of claim 1, "a N-well" should be changed to --an N-well--. Note that claims 2-8 are objected to because they include the informality of claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Shigehara et al. (USP 6,084,431).

With respect to claim 1, Figure 10 of the Shigehara et al. reference discloses a buffer, which includes: an I/O circuit (P1, N1, N11) comprising a first PMOS (P1) having an N-well (Nwell), a first NMOS (N1), a first gate control signal (output of NOR1), an I/O pad (IO); a P-gate control circuit (P2, P3, P7, N12, N2, N3); a feedback detection device (P11, P12, N14) for providing a feedback signal (IO/); system voltage (Vcc); and an N-well control circuit (12, P8, N13, N4, P9, P6, P4, N13, N14, N5, P6, P9 and the PMOS connected between P4 and node IO).

With respect to claim 2, it is seen in the operation of the circuit in Figure 6 that the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor (P1) to the voltage level of the input voltage (IO) when the input voltage (IO) exceeds the system voltage (line 66 of Col. 10 to line 14 of Col. 11. Note that "terminal 10" on line 8 of Col. 11 actually is --terminal IO--).

With respect to claim 3, it is seen in the operation of the circuit in Figure 6 that the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor (P1) to the system voltage (Vcc) when the input voltage (IO) is lower than the system voltage (when the voltage at input IO is low, PMOS transistor P4 turns on so that the Nwell has a voltage of Vcc).

With respect to claim 4, Figure 10 shows the second NMOS (N11).

With respect to claim 7, Figure 6 shows the feedback detection device (P11, P12, N14) is an inverter.

Allowable Subject Matter

5. Claims 9 and 10 are allowed.

Claim 8 is allowed because the prior art of record fails to disclose or suggest a buffer including first to fifth NMOS transistors, first to sixth PMOS transistors, and an N-well with the recited connections set forth therein.

Claim 9 is allowed because it depends on claim 8.

6. Claims 5, 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 would be allowed because the prior art of record fails to disclose or suggest that the N-well control circuit of the buffer including second to fourth PMOS transistors, and third and fourth NMOS transistors with the recited connections set forth therein.

Claim 6 would be allowed because it depends on claim 5.

Claim 8 would be allowed because the detection inverter of the buffer including a sixth NMOS, a seventh PMOS and a seventh NMOS with the recited connections set forth therein.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 13, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816